Assignment - 2.

Module 2

1] Explain various currents flowing through the BJT transistor.

→ i) Emitter current:
- Total current flowing into the emitter terminal of BJT.
- It is the sum of base and collector currents in an ideal transistor ($I_E = I_B + I_C$).
- $I_E$ is approx equal to $I_C$ because the base current is small compared to $I_C$

ii) Collector current:
- Current flowing through the collector terminal of BJT.
- It is controlled by the base current ($I_B$) and is typically in the milliampere (mA) range.
- In an NPN transistor, when $I_B$ allows electron flow, a larger $I_C$ flows from the collector to emitter.
- In an PNP transistor, $I_C$ flows from emitter to the collector when $I_B$ allows hole flow.

iii) Base current:
- Current flowing into the base terminal of BJT
- It controls the transistor's operation and typically in uA range
- For NPN transistor, $I_B$ allows electron flow from emitter to base
- For PNP transistor, $I_B$ allows hole flow from the emitter to the base.

2] Explain the transistor biasing circuit with relevant explanation.

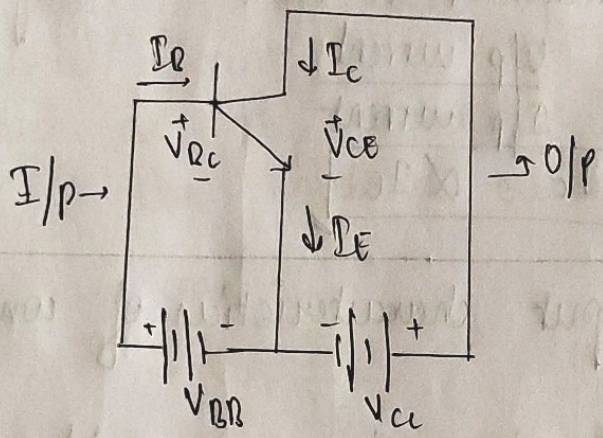
→ • Transistor Biasing: Ensures a transistor operates in the desired region for amplification.
- Fixed Bias circuit:
- Uses resistors to ~~explain~~ set base voltage ($V_b$).
- Collector voltage ($V_c$) connects through a resistor ($R_c$) to supply voltage ($V_{cc}$).

Self-bias Circuit:

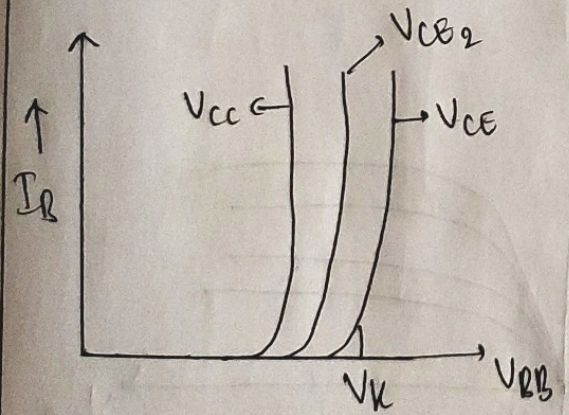
- Relies on the voltage across an emitter resistor ($R_e$) for base biasing.
- Base voltage ($V_b$) is determined by $R_e$ and base-emitter voltage ($V_{be}$).

3] Explain input and output characteristics of common emitter configuration.

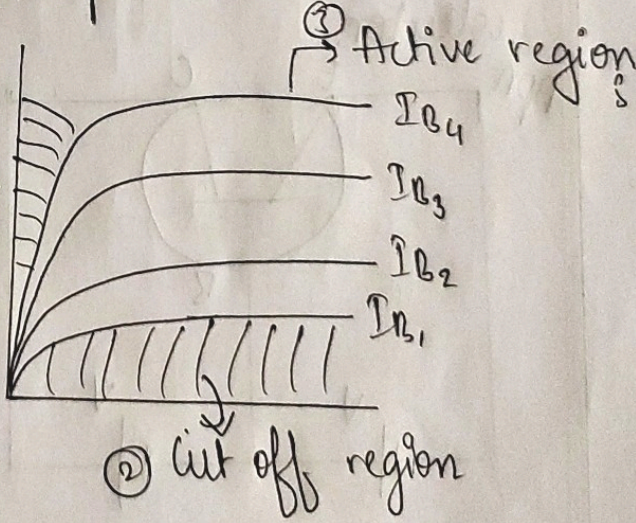
→ Common-emitter




Input character




Output characteristics:




It provide 3 different regions:

1. Saturation: In this region base & emitter must be forward bias and collector and emitter also to be forward bias. It gives max collector current ($I_c$).

2] Cut off: In this region base emitter is in reversed bias and collector and emitter also to be reversed bias. When BE is reversed bias $I_B = 0$. Current gain $= \beta = \frac{\text{Output Current}}{\text{Input Current}}$

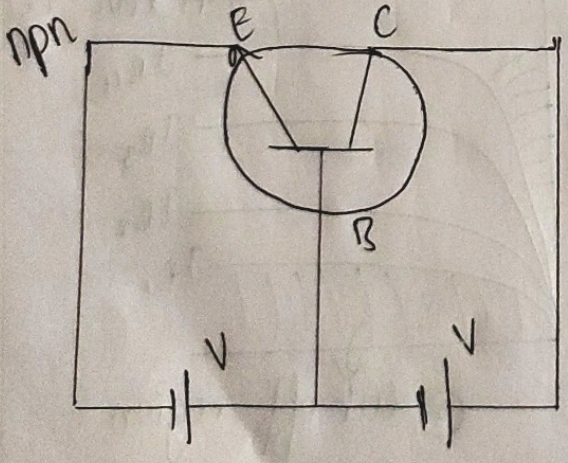
3] Active region: In this region base emitter is in forward bias and collector emitter is in reversed bias. In this region transistor is used as amplifier

$$\alpha = \frac{\text{O/P current}}{\text{I/P current}}$$

$$\boxed{I_C = \alpha I_E}$$

4] Explain input output characteristics of common base configuration

→ Common-base: The base is common b/w emitter and collector.

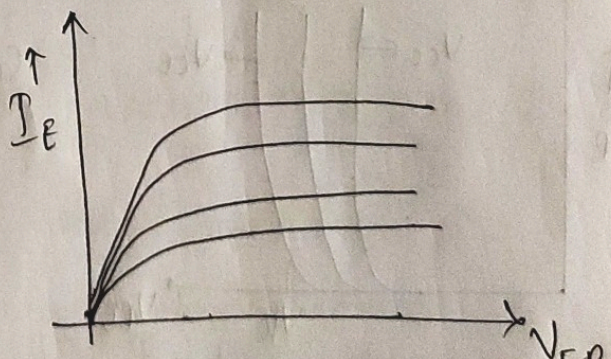



$I_E = I_B + I_C$

MA MA MA

$I_B = 0$

$I_E = I_C$




I/P current = $I_E$

I/P voltage = $V_{EB}$

$$\boxed{\text{O/P} = V_{BC} \text{ \& } I_C}$$

O/P & I/P values are in phase

In case of common-base configuration the current gain is

$$\alpha = \frac{\text{O/p current}}{\text{I/p current}}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\boxed{I_C = \alpha I_E}$$

$\alpha = 0.9 \sim 1$ → Theory

↓ practical

5] Define $\alpha$ & $\beta$. Determine relationship between $\alpha$ & $\beta$.

→ $\alpha$ is defined as the ratio of the collector current to the emitter current.

$\beta$ is defined as the current gain which is given by the ratio of the collector current to base current.

Relation b/w $\alpha$ and $\beta$

$$\beta = \frac{I_C}{I_B} \qquad \alpha = \frac{I_C}{I_E} \qquad I_E = I_C + I_B$$

$$\alpha = \frac{I_C}{I_E}$$

$$= \frac{I_C}{I_C + I_B}$$

Divide Numerator & Denominator by $I_B$

$$= \frac{I_C/I_B}{I_C/I_B + I_B/I_B}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

Why $\beta = \frac{I_C}{I_B}$

$$= \frac{I_C/I_E}{I_E/I_C - I_C/I_E}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

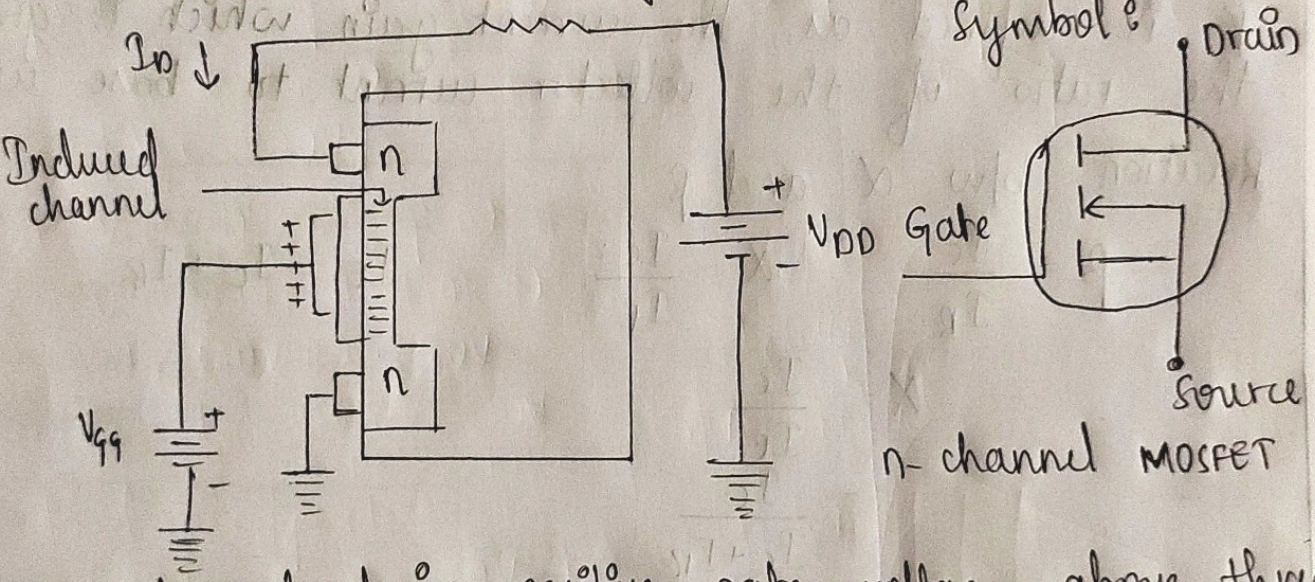
$V_{in}$ $V_o = \frac{\quad}{\quad} \cdot V_{in}$

6] Make use of N-channel enhancement type MOSFET and describe the construction & working

→ MOSFET is different from JFET has no pn junction instead gate is insulated from channel by silicon dioxide ($SiO_2$).

Enhancement MOSFET

- It operates in enhancement mode, has no depletion region
- The construction of n-channel enhancement mode MOSFET is shown below. Here n regions are defused into p-type substrate using diffusion process.

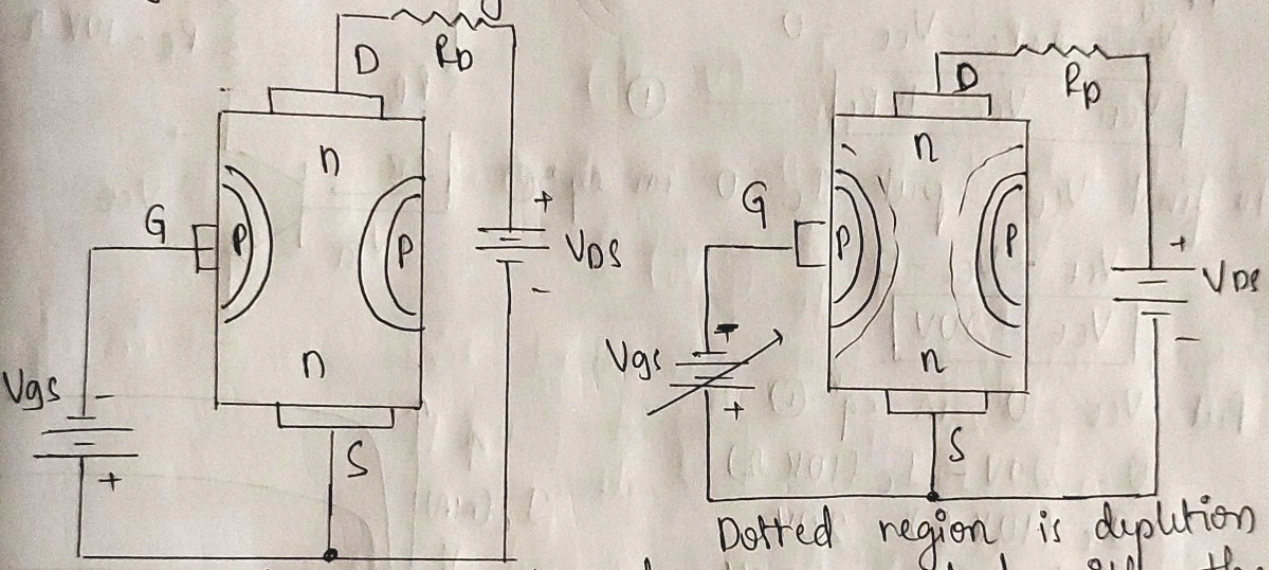



- For n-channel device, positive gate voltage above threshold voltage induced channel by creating thin layer of negative charges in the substrate region. ie adjucent to $SiO_2$ layer conductivity of this channel is enhanced by increased gate to source voltage and hence it pulls more electrons into the channel
- Gate voltage below threshold no channel created

1] Make use of n-channel JFET to describe its operation & characteristics.

→ Operation:

To illustrate operation of JFET, the fig below shows dc bias voltage applied to an n-channel device. $V_{DS}$ provides a drain to source voltage and supplies current from drain to source. $V_{GS}$ set reverse bias voltage between gate & source




Dotted region is depletion region

Case a: The JFET is always operated with the gate to source junction reverse biased. The reverse biasing of G-S with negative voltage produces a depletion region along pn-junction, and extend in n-channel Hence, increase in resistance by restricting channel

Case b: As voltage across gate & source increases, depletion region created by reverse bias increases and narrows the channel which increases the resistance of the channel and decreases $I_D$.

NOTE: Distance b/w dotted lines decreases.

Case c: As voltage across $V_{GS}$ decreases, depletion region created by reverse bias decreases and widens the channel which decreases the resistance of the channel and Increase $I_d$.

NOTE: Distance b/w dotted lines increases.

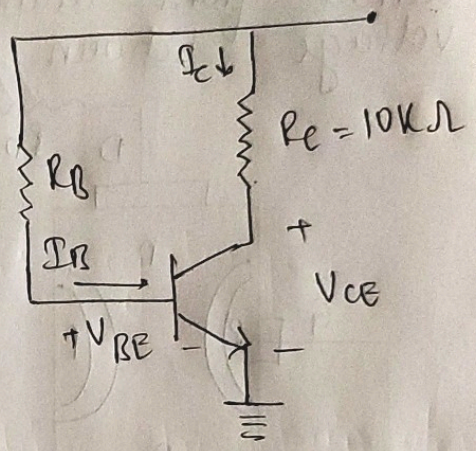
Characteristics:
- Voltage- controlled
- High input Impedence
- Low Noise
- Temperature sensitive

8] Draw the DC load line for circuit shown.

→ Apply KVL to collector emitter,

$V_{cc} - I_c R_c - V_{CE} = 0$

$\boxed{V_{CE} = V_{cc} - I_c R_c}$ —— ①




To find $V_{CE}$, put $I_c = 0$ in eqn ①

$V_{CE} = V_{cc} - 0$

$\boxed{V_{CE} = 20V}$

Put $V_{CE} = 0$ in eqn ①

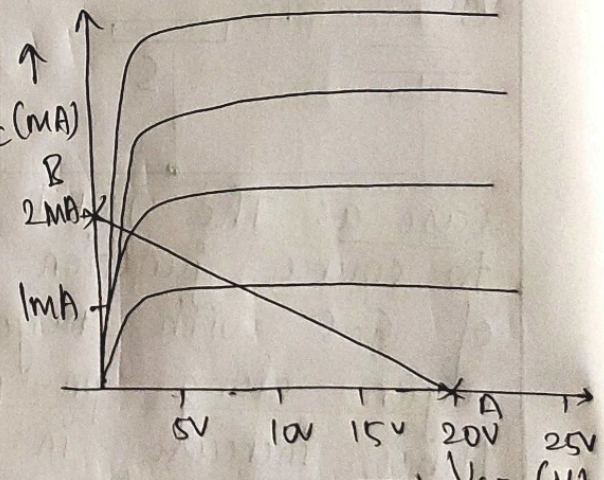
$0 = 20V - I_c (10K\Omega)$

$I_c (10K\Omega) = 20V$

$I_c = \frac{V_{cc}}{R_c} = \frac{20V}{10K\Omega} = 2mA.$

DC load line points:

$\boxed{\begin{array}{l} 1)\ I_c = 0,\ V_{CE} = 20V \\ 2)\ V_{CE} = 0,\ I_c = 2mA \end{array}}$




9] Calculate the values of $I_c$, $I_E$ and $\beta_{dc}$ for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 100A$.

→

* $\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} = 49$

* $I_c = \beta_{dc} I_B = 49 \times 100 = 4900A$,

Module 3

10] Briefly discuss ideal characteristics of Op Amp.

→ i) Common mode rejection ratio-
It is ratio of differential mode gain to the common mode gain.
ie. $CMRR = \frac{A_{DM}}{A_{CM}}$

2] Output offset voltage - The actual o/p when i/p of op amp is zero is called output offset voltage

3] Input offset voltage - Because of unavoidable inbalance inside the op amp a small voltage is been applied b/w the i/p terminals that make o/p is zero.

4] I/p resistance - It is measured b/w inverting & non-inverting terminal due to this it will not allow to draw current from voltage source (∞ ideally).

5] O/p resistance - The resistance is measured b/w the o/p terminal of op amp & ground (0 ideally).

6] Slew rate - It is defined as how fast the o/p of op amp can change to the change in i/p ie the max rate at which the o/p can change

7] Open loop & closed loop configuration -
. In case of open loop the o/p is directly proportional to i/p with some proportionality constant.
. In case of closed loop the feedback structure is existing & this will control the system. It provides stabled system with less gain factor.

---

11] Derive an expression for integrator.

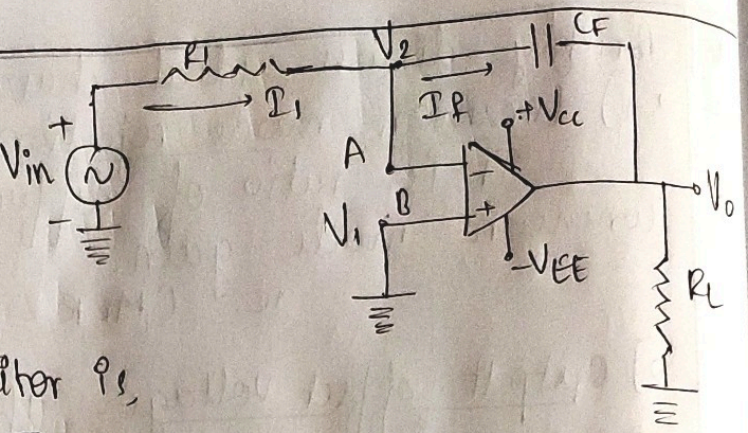
→ A circuit in which the o/p voltage waveform is the integral of i/p voltage waveform is called Integrator.

KCL at node ② ie $V_2$,

$$i_1 = i_B + i_f \quad \text{—— ①}$$

since $I_B$ is small.

$$I_1 \cong I_f \quad \text{—— ②}$$




The current through capacitor is,

$$i_c = C_f \frac{dV_c}{dt} \quad \text{—— ③}$$

$$\frac{V_{in} - V_2}{R_1} = C_f \frac{d}{dt}(V_2 - V_o)$$

W.K.T $V_1 = V_2 \approx 0$ because A is very large.

$$\therefore \frac{V_{in}}{R_1} = C_f \frac{d}{dt}(-V_o)$$

Now integrate both side w.r.t time to obtain o/p voltage

$$\int_0^t \frac{V_{in}}{R_1} dt = \int_0^t C_f \frac{d}{dt}(-V_o)\, dt$$

$$\frac{1}{R_1}\int_0^t V_{in}\, dt = -C_f \int_0^t \frac{d}{dt}(V_o)\, dt$$

$$\boxed{V_o = -\frac{1}{R_1 C_f}\int_0^t V_{in}\, dt + C}$$

12] Device an expression for 3 input summing circuit.

→ $I = I_1 + I_2 + I_3$

$I = I' + I_f$

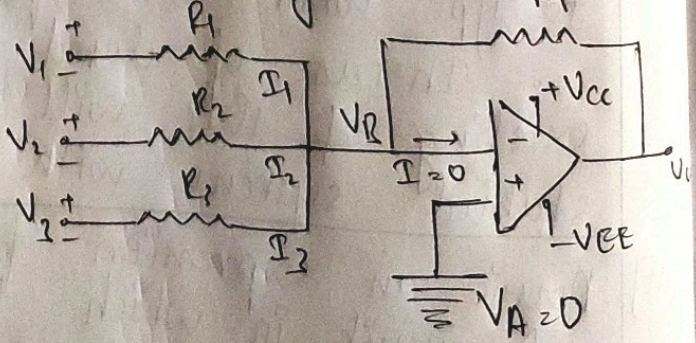
$I = I_f$

$I_f = (I_1 + I_2 + I_3)$

Let $R_1 = R_2 = R_3 = R_f$.

$V_B - V_f - V_o = 0$

$V_B - V_o = I_f R_f$



$$\frac{-V_0}{R_f} = I_f \qquad I_1 = \frac{V_1 - V_R}{R_1} \qquad I_2 = \frac{V_2 - V_R}{R_2}$$

$$\frac{-V_0}{R_f} = I_1 + I_2 + I_3$$

$$-\frac{V_0}{R_f} = \frac{+V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \qquad (R_1 = R_2 = R_3 = R_f)$$

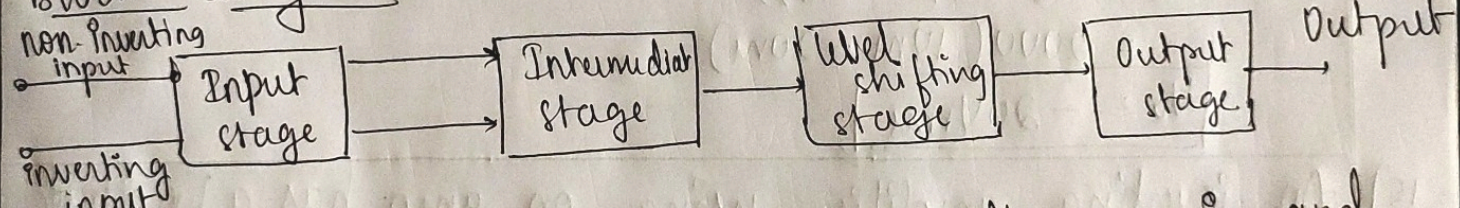
$$-V_0 = V_1 + V_2 + V_3$$

$$\boxed{V_0 = -(V_1 + V_2 + V_3)}$$

13] Explain with a neat block diagram of an Op-Amp.

→ An operational amplifier is a direct coupled high-gain amplifier consisting of one or more differential amplifier used to amplify AC and DC signals.

Block diagram :-




* Input stage : Provides most of the voltage gain and establishes input resistance

* Intermediate stage :
- driven by the output of first stage
- o/p level of intermediate stage is above ground as direct coupling is used

* level stage :
- level shifting stage is used to shift the o/p of intermediate stage downward.

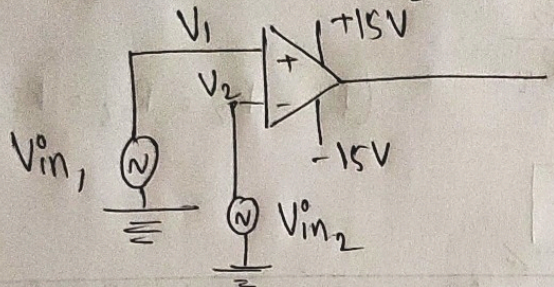
* Output stage :
- increases the o/p voltage swing
- raises the current supplying capability
- provides low o/p resistance

14] Determine the o/p voltage in each of the following cases for the open-loop differential amplifier

a) $V_{in_1} = 5V$ dc, $V_{in_2} = -7V$ dc

b) $V_{in_1} = 10mV$, $V_{in_2} = 20mV$

→




(a) W.K.T $V_o = A(V_{in_1} - V_{in_2})$

$= 2000(5 - (-7))$

$\boxed{V_o = 24000V}$

(b) $V_o = A(V_{in_1} - V_{in_2})$

$= 2000(10m - 20m)$

$\boxed{V_o = -20V_{rms}}$

15] An inverting amplifier using op-amp has a feedback resistor of 10k calculate the gain of op amp & o/p voltage if it supplied with an input 0.5V

→ Given, $R_f = 10K\Omega$, $R_1 = 1K\Omega$, $A = ?$, $V_o = ?$, $V_{in} = 0.5V$

$A_v = \frac{-R_f}{R_1} = \frac{-10K}{1K}$

$\boxed{A_v = -10}$

Inverting amplifier

$V_o = -A \cdot V_{in}$

$A_v = \frac{R_f}{R_1}$

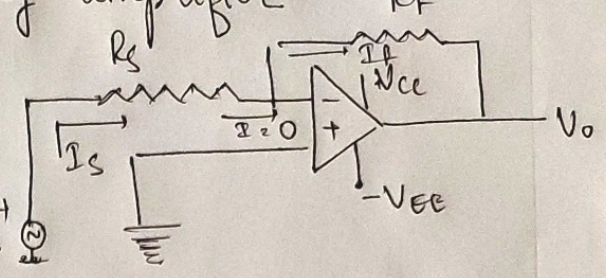
$V_o = -\frac{R_f}{R_1} V_{in}$

$V_o = \frac{-10K}{1K} 0.5$

$\boxed{V_o = -5V}$

16] Derive voltage gain for inverting amplifier

→ An amplifier which produces a phase shift of 180° between i/p & o/p is called inverting amplifier




In this circuit,

$$I_s = I + I_f$$

$$\boxed{I_s = I_f} \quad \text{— (1) At } I_i = 0$$

$V_1$ = Ground = 0

$V_1 = V_2 = 0$

$V_1 - V_2 = V_d$

W.K.T. $\quad I = \dfrac{V_1 - V_2}{R}$

Now $\quad I_s = \dfrac{V_{in} - V_2}{R_s}$ — (2)

$$I_f = \frac{V_2 - V_o}{R_f} \quad \text{— (3)}$$

Put (2) & (3) in eqn (1)

$$I_s = \frac{V_{in}}{R_s} \qquad I_f = \frac{-V_o}{R_f}$$

$$I_s = I_f$$

$$\frac{V_{in}}{R_s} = \frac{-V_o}{R_f}$$

$$\boxed{V_o = -\frac{R_f}{R_s} \cdot V_{in}}$$

Here, Gain = $A = \dfrac{R_f}{R_s}$

$$\therefore \boxed{V_o = -A \cdot V_{in}}$$

Rf $\quad \boxed{V_o = -\frac{R_f}{} A \cdot V_{in}}$