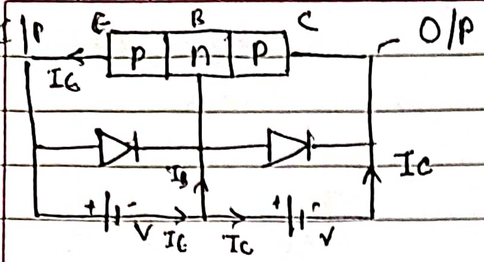
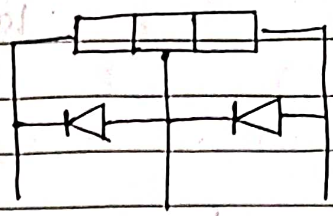
Module - 3

14/5/24

BIPOLAR IN TRANSISTOR

①




- The transistor defined as transfering the signal from low resistance [forward bias] as a input] to high resistance [reverse bias as a output].

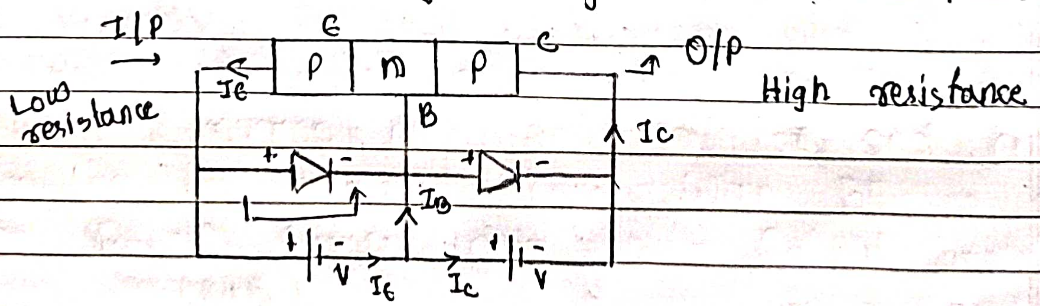
- There are two types of transistor
  (i) p-n-p (ii) n-p-n

- Transistor having 3 terminals namely emitter, base and collector

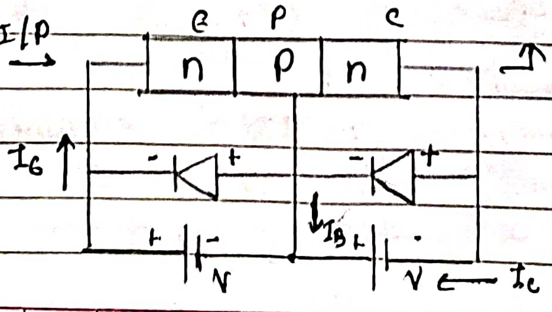
- Emitter : It emittes or inject majority charge carriers [e^- or holes] hence it is highly doped.

- base : It allows to bi-pass majority charge carriers.

- Collector : It is moderately doped and collects all the majority charge carriers of emitters.

①


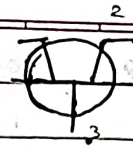
$$I_E = I_B + I_C$$

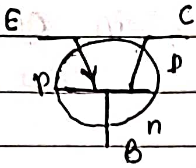
②


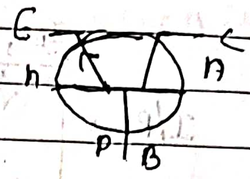
BE → FB → I/P	
BC → RB → O/P	

$$I_B + I_C = I_E$$

- Symbol of transistor







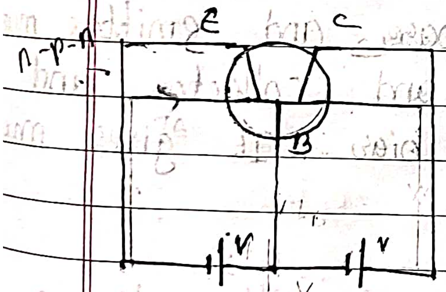
If comming to the base then p type
E ⇌ C

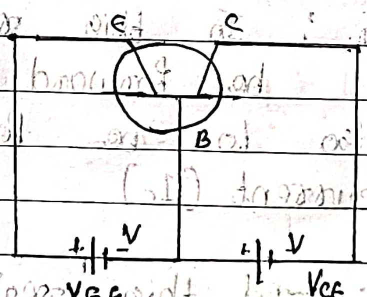
leving base then n type
E ⇌ C

* Types of configuration :
Based on requirement of current gain or high impedence the transistor configured as

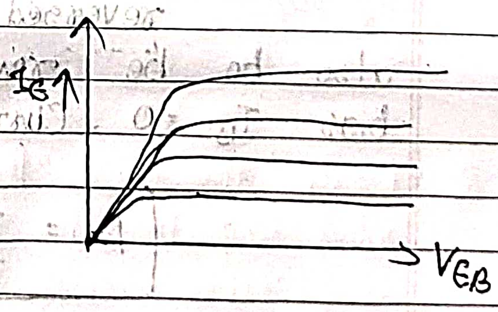
i] C-B Configuration
ii] CE "
iii] CC "

* Common Base [CB] :- The base is common b/w emitter and collector





mA µA mA
$I_E = I_B + I_C$
↳ negligible
$I_B = 0$
$I_E = I_C$

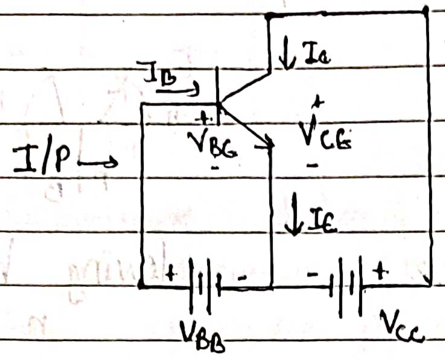


O/P = V_{BC} & I_C

I/P Current = I_E
" voltage = V_{EB}

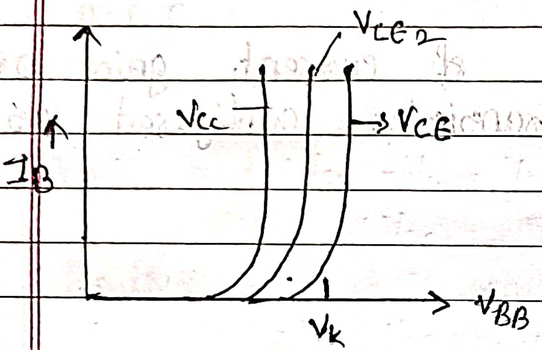
O/P & I/P values are in phase

* Common - Emitter

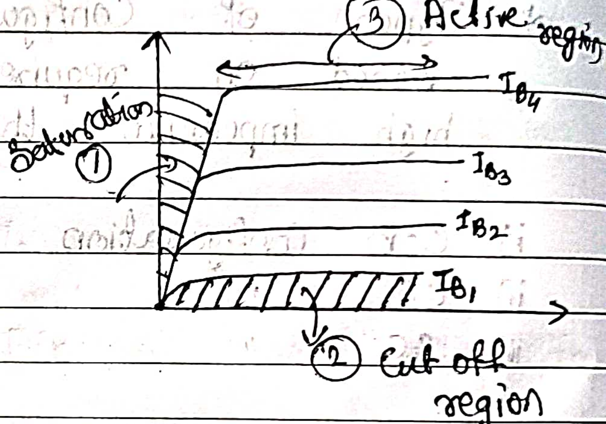


I/P & O/P are in out of phase

Input character



Output character



Output Characteristics

- It provide 3 different regions

1 Saturation : In this region base and emitter must be forward bias and collector and emitter also to be forward bias. It gives max collector current (I_c)

2 Cut off :- In this region base emitter is in reversed bias and collector and emitter also to be reversed bias. When BE is reversed bias $I_B = 0$. Current gain $= \beta = \frac{\text{Output Current}}{\text{Input Current}} =$

$$\boxed{\beta = \frac{I_c}{I_B}}$$

$\beta = 100$ ↓ Theoritical ~ 100 ↳ practical

$\therefore I_c = \beta I_B$

$I_B = 0$

$$\boxed{I_C = 0}$$

In this region the transistor is used as '**switch**'

3 Active : In this region base emitter is in forward bias and collector emitter is in reversed bias. In this region transistor is used as amplifier.

In case of common-Base configuration the current gain is 'α' = O/P current / I/P current

$$\alpha = \frac{I_C}{I_E}$$

α = 0.9 ~ 1
↓ practical ↳ Theory

$$\boxed{I_C = \alpha I_E}$$

* Relation b/w α and β

$$\beta = \frac{I_C}{I_B} \qquad \alpha = \frac{I_C}{I_E} \qquad I_E = I_C + I_B$$

$$\alpha = \frac{I_C}{I_E} = \frac{I_C}{I_C + I_B}$$

Divide numerator & denomenator by I_B

$$= \frac{I_C/I_B}{I_C/I_B + I_B/I_B}$$

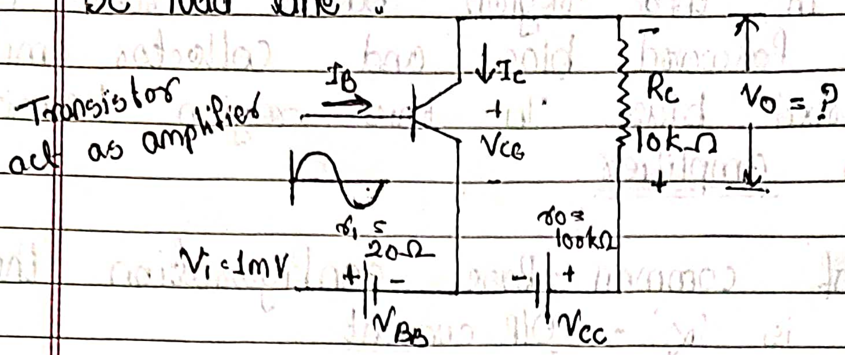
$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

Ily $\beta = \frac{I_C}{I_B}$

$$= \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

- DC load line :



* Finding the max collector current and max collector emitter voltage is called DC load line.
To obtain DC load line apply KVL to the output of the given circuit.

$$+V_{CC} - V_o - V_{CE} = 0$$

$$V_{CE} = V_{CC} - V_o$$

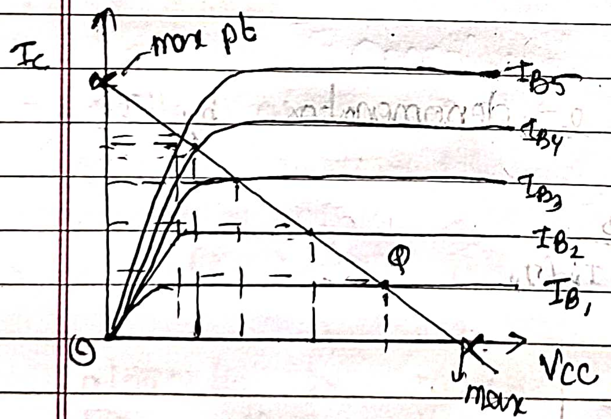
$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad \text{— (1)} \quad \text{[standard eqn]}$$

(1) $I_C = 0$

$$\boxed{V_{CE_{max}} = V_{CC}}$$

(2) $V_{CE} = 0$

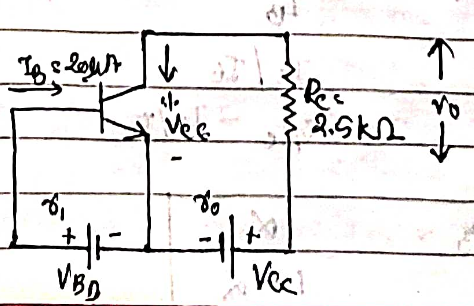
$$\boxed{I_C = \frac{V_{CC}}{R_C}}$$

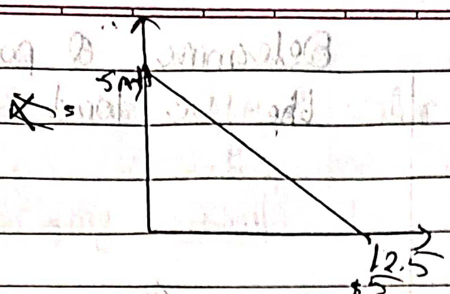


Q = Stable point

Q Draw the DC load line if $V_{CC} = 12.5$, $R_C = 2.5k\Omega$ what will be the Q point if $I_B = 20\mu A$ and $\alpha = 0.99$

→





$I_C = \frac{V_{CC}}{R_C} = \frac{12.5}{2.5 \times 10^3}$

$I_C = 5mA$

$I_B = 20\mu A$, $I_C = 5mA$

$\beta = \frac{\alpha}{1-\alpha}$

$= \frac{0.99}{1-0.99}$

$\beta = 99$

$\beta = \frac{I_C}{I_B}$

$99 = \frac{5 \times 10^{-3}}{I_B \; 20 \times 10^{-6}}$

$I_B = 99 \;\; 5 \times 10$

$99 \times 20 \times 10^{-6} = I_C$

$I_C = 1.98 \times 10^{-3}$ A

$I_C R_C \;\; V_{CC}$

$1.98 \times 10^{-3} \times 2.5 = V_{CC}$

$V_{CC} = 4.95 \times 10^{-3}$

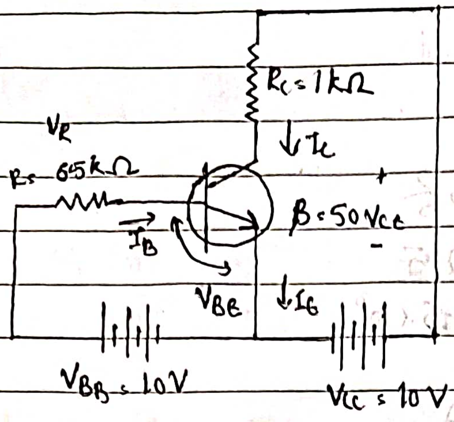
$V_{CE} = 12.5 - 1.98 \times 2.5 \times 10^{-3}$

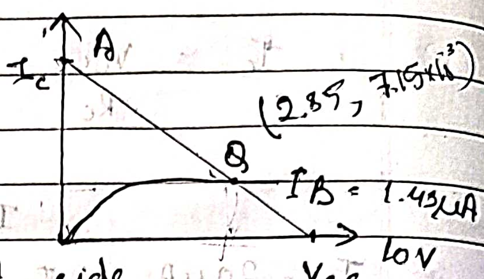
$= 12.5 - 4.95 \times 10^{-3}$

$V_{CE} = 12.495$

$Q_e = 0.3$

(2) Determine Q point and Draw the DC load, silicon transistor





→ By applying KVL on output side

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$I_C = 0$

$$V_{CE} = V_{CC}$$

$$V_{CE} = 10\ V$$

$$0 = V_{CC} - I_C R_C$$

$$\frac{V_{CC}}{R_C} = I_C$$

$$\frac{10}{1000} = I_C$$

$$I_C = 0.01\ A$$

$$\beta = \frac{I_C}{I_B} \qquad I_B = \frac{I_C}{\beta}$$

$$= \frac{10\times10^{-3}}{50}$$

$$= 2\times10^{-4}$$

$$I_B = \frac{V}{R_B}$$

$$= \frac{10 - 0.7}{65\times10^3}$$

$$I_B = 1.430\times10^{-4}\ A$$

$$= 143\ \mu A$$

KVL

$$V_{BB} - V_R - V_{BE} = 0$$

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$10 - I_B(65\times10^3) - 0.7 = 0$$

$$+ I_B(65\times10^3) = 9.3$$

$$I_B = \frac{9.3}{65\times10^3}$$

To Determine the value of Q point we need to identify the base current (Input current) by applying KVL to input side.

$V_{CE} = V_{CC} - I_C R_C$
$= 10 - (7.15 \times 10^{-3})(1 \times 10^{3})$
$= 10 - 0.143$
$= 9.857$ V
$V_{CE} = 2.85$ V

$\beta = \frac{I_C}{I_B}$

$50 \times 143 \times 10^{-6} = I_C$

$7.15 \times 10^{-3} = I_C$

* Need of Biasing :
- To maintain proper zero signalling
- To maintain proper V_{BE} and V_{CE}.

* The collector current should ~~cha~~ not change its position [Operating pt]. But the operating pt suppose to be change due to base current hence the proper design has to be established

* Note :- In Case of CE the output signal is amplified but their is a phase shift w.r.to input signal.

In case of CB the output signal is inphase w.r.to input signal [amplification is based on resistor].